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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,370	05/18/2005	Wolfgang Buhr	DE02 0274 US	1614

65913 7590 10/09/2007

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EXAMINER	
KHUU, HIEN DIEU THI	
ART UNIT	**PAPER NUMBER**
2863	

NOTIFICATION DATE	DELIVERY MODE
10/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/535,370	BUHR, WOLFGANG	
	Examiner	Art Unit	
	Cindy D. Khuu	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 11-16* is/are pending in the application.

4a) Of the above claim(s) *11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/14/2007 has been entered.

Response to Applicant's Election/Restrictions

Claims 11-16 were originally withdrawn from consideration as being directed to a non-elected invention, according to office action dated 5/17/2007. Applicant's amendment to claim 16 dated 9/14/2007, is now considered and claim 16 has been rejoined for examination. However, Examiner maintains the position to withdraw claims 11-15 for the reason stated in office action dated 5/17/2007.

Claim Objections

Claim 16 is objected to because of the following informality: The following underlined limitations do not correlate to the disclosure and are unclear: ***a code ROM module interface logic circuit for receiving an address from said microcontroller*** (examiner believes Applicant meant to claim "from said CPU"); ***receiving an encrypted memory module address from a CPU and data from said microcontroller*** (applicant claims microcontroller comprises a security controller circuit which includes CPU, ROM, NVM, etc., hence underlined limitation is unnecessary); ***storing said encrypted data in said decrypted memory module address of said non-volatile memory*** (examiner is unclear and cannot correlate to Applicant's disclosure).

Claim 1 is objected to because of the following informality: The following underlined limitation does not correlate to the disclosure and is unclear: ***said at least one ROM code further being used for***

decrypting a memory module address coming from a CPU (examiner is unclear and cannot correlate the underlining limitation to what have been disclosed in paragraphs 0041-0042; it has been disclosed that --the ROM code is used as an en-/decryption key for encryption or decryption of the address data from the CPU--; it has not been disclosed that "the ROM code used for decrypting a memory module address coming from a CPU).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Kocher et al. (US 6,289,455).

With respect to claim 1, Kocher discloses a circuit arrangement for electronic data processing comprising (Fig. 2):

at least one non-volatile memory module (265) for storing encrypted data to be protected against unauthorized access (Column 9, lines 40-41);

at least one memory module interface logic circuit (260) in electronic communication with the memory module (Fig. 2); said at least one memory module interface circuit being for addressing the memory module, for writing the data to the memory module, or for reading out the data from the memory module (Column 9, lines 40-41);

at least one code Read Only Memory (ROM) module (245) for storing and/or supplying at least one ROM code (Column 9, line 33); and

at least one code ROM module interface logic circuit (240-225-200) in electronic communication with the code ROM module (Fig. 2) for addressing the code ROM module and for reading out the ROM code from the code ROM module (Column 9, lines 28-41),

wherein the at least one ROM code stored in the code ROM module (Column 9, line 33) is used to generate at least one key code for encrypting or decrypting data being written to the memory module or data being read from the memory module (Column 10, lines 46-47), said at least one ROM code further being used for decrypting a memory module address coming from a central processing unit (see objections above; examiner interprets that a code being used to decrypt *address data* from a CPU; hence Column 11, lines 33-65 of Kocher discloses the limitation; examiner sees that Kocher discloses a decryption of content that is stored in an address location in the protected memory, column 11, lines 44 and 65, and ICP sends both the address in the protected memory and the content decryption key to the cryptofirewall to decrypt the content step 590).

With respect to claim 2, Kocher further discloses a circuit arrangement wherein the memory module interface logic circuit comprises at least one en-/decryption logic circuit (260) having at least one key address generation unit for generating a ROM key address (valid key offset) using a *memory module address* coming from the CPU (address from the ICP; column 16, line 54) and having at least one key register (Column 16, lines 50-60).

With respect to claim 3, Kocher further discloses a circuit arrangement wherein the code ROM module interface logic circuit comprises at least one multiplexing unit (Column 9, line 3).

With respect to claim 4, Kocher further discloses a circuit arrangement wherein the memory module takes the form of at least one electrical erasable programmable read only memory (Column 10, line 39) or at least one Flash memory (Column 25, line 61).

With respect to claim 5, Kocher further discloses at least one circuit arrangement, comprising a microcontroller (225), in particular an "embedded security controller" (Column 21, lines 7-10).

With respect to claim 16, Kocher further discloses a microcontroller (225) comprising a security controller circuit (Column 21, lines 7-10), said security controller circuit comprising:

a non-volatile memory (265) for storing encrypted data (Column 9, lines 40-41);

a memory module interface logic circuit (260) for reading and writing encrypted data to and from said non-volatile memory (Column 9, lines 40-41);

a code ROM (245) for storing a plurality of key codes (Column 9, line 33; column 10, lines 36-47); and a code ROM module interface logic circuit for receiving an address from said *microcontroller*, for using said address to read a key code from said code ROM, and for providing said key code to said memory module interface logic circuit (column 11, line 45; column 16, line 53);

said memory module interface logic circuit (260) being further for receiving an encrypted memory module address from a central processing unit (column 16, lines 52-54) and *data from said microcontroller*, for using said key code to decrypt said encrypted memory module address (Column 10, lines 46-47), *for encrypting said data*, and for storing said encrypted data in said *decrypted* memory module address of said non-volatile memory (column 10, lines 65-67).

Response to Arguments

Applicant's amendment and arguments filed 09/14/2007 have been fully considered but they are not persuasive.

During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification. In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969)

Regarding the 35 U.S.C. 102(b) rejections, Applicant argues that Kocher does not disclose at least one ROM code further being used for decrypting a memory module address coming from a central processing unit.

Examiner's position is that Kocher discloses at least one ROM code further being used for decrypting a memory module address coming from a central processing unit (Column 11, lines 33-65). Paragraphs 0041 and 0042 of Applicant's disclosure, describes a code being used to decrypt *address data* from a CPU. Therefore, Kocher discloses a decryption of content that is stored in an address location in the protected memory and ICP sends both the address in the protected memory and the content decryption key to the cryptofirewall to decrypt the content (step 590 and column 11, lines 44 and 65).

Applicant further argues that Kocher does not disclose cryptographically modifying the memory module addresses that are used to write data to or read data from the protected memory.

Examiner's position is that Kocher clearly discloses the encryption and decryption of data content being read and write from the protected memory (figure 5, step 590; column 10, lines 5-25; column 11, lines 33-65; column 16, lines 47-67; and column 17, lines 1-20).

Fax/Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cindy D. Khuu whose telephone number is (571) 272-8585. The examiner can normally be reached on M-F, 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CMW 9/28/07

John Barlow
Supervisory Patent Examiner
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